28.4 A CMOS Image Sensor with a Column-Level Multiple-Ramp Single-Slope ADC

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This paper presents a CMOS image sensor that uses a column-level ADC with a new multiple-ramp single-slope (MRSS) architecture. At similar power consumption, this architecture achieves a 3.3× reduction in A/D conversion time compared with the classical single-slope architecture. Like the single-slope ADC, the MRSS ADC requires only a single comparator per column, and, additionally, 8 switches and some digital circuitry. A prototype has been realized in a 0.25µm CMOS process. Measurements show that compared to an imager with a single-slope ADC, the MRSS ADC enables a frame rate increase of 2.8× while dissipating only 24% more power.

In recent years, column-level ADCs have become quite common in CMOS image sensors [1, 2] because a large number of parallel ADC channels are used, which facilitates the high speed readout of large pixel arrays. Column-level ADCs usually employ a single-slope architecture, which has the advantage of requiring only one comparator per column. Such simple column circuitry reduces the required chip area and makes it relatively easy to ensure uniformity between column circuits. However, a disadvantage of the single-slope architecture is the fact that its conversion time increases exponentially with the number of bits, which limits read-out speed at high resolutions [2]. While successive approximation or algorithmic ADCs are much faster, these all require much more in-column circuitry, which increases chip area, layout complexity and column non-uniformity.

The MRSS ADC achieves a significantly lower conversion time while preserving the key benefit of the single-slope ADC, its simple column circuitry. Figure 28.4.1 shows the block and timing diagrams of an MRSS ADC. The column circuitry consists of a single comparator that can be connected to several ramp voltages, labeled 1 through m. An A/D conversion is divided into a coarse and a fine conversion phase. During the coarse phase, all comparators are connected to the first ramp, and a single-slope conversion of $m=2^p$ clock periods is performed, which provides a coarse (p-bit) approximation of the input signal. In the fine A/D conversion phase, all m ramps are operated concurrently for 2^q clock periods, with each ramp spanning $1/m$ times the range of the coarse ramp. Based on the results of the coarse phase, each comparator is connected to the appropriate ramp. The number of clock periods required for a complete conversion is therefore $2^p + 2^q$, where $p + q$ is the ADC's resolution. The choice of p and q involves a design trade-off between power (dissipated in the ramp generators) and speed. In this design, 8 ramps were selected, resulting in $p = 3$ and $q = 7$ for 10b resolution. To prevent the creation of dead-bands, the implemented ramp voltages overlap each other somewhat.

Figure 28.4.2 shows the implemented column-level ADC circuit. The comparator is similar to that presented in [1, 2] and is re-used from an existing design. It is auto-zeroed using capacitor C1 and switch S2. During the auto-zero phase, the output of the column-level CDS amplifier is also sampled on C1. Next, the comparator is connected to one of the ramp voltages via S3. During the coarse ADC phase, ramp1 outputs a coarse ramp that is input into each comparator by using the control line *force_ramp1*. The result of the coarse A/D conversion is stored in 3 bits of the column memory, and is subsequently fed into a 3-to-8 decoder that connects the comparator to the correct ramp. After this, the fine A/D conversion phase is performed, the results of which are stored in the other 8 bits of the column memory.

In Fig. 28.4.3, a block diagram of the ramp generator is shown. The ramps are generated by 8 12b resistor-ladder DACs [3]. For correct operation of the MRSS architecture, it is imperative that the slopes of the ramps match well and that their offsets are well-defined. This is achieved by using a single coarse resistor ladder, to which 8 fine resistor ladders are connected to generate the ramp voltages. With a proper choice of resistor values, it is not necessary to use buffer amplifiers between the coarse and fine ladders. To compensate for the switch resistance, the fine ladder uses NMOS transistors (T_2 through T_{31}) as resistors that are matched to the force switches T_1 and T_{32} between the coarse and fine ladders. A separate set of sense switches is used to directly output the voltage at the coarse resistor nodes. The DAC outputs are buffered by folded-cascode opamps, which drive the column circuitry. Their offset variations are compensated by a digital auto-calibration algorithm involving a test-column, whose comparator is connected to ramp1. While the pixel voltages are output to the front-end CDS amplifiers, ramp1 feeds in test voltages corresponding to the middle of one of the other ramps to the test comparator, which subsequently performs the same A/D conversion as the other columns. The digital output of the test column contains the offset of one of the ramps compared to ramp1. This is averaged and subsequently cancelled in the digital domain, simply by changing the code assigned to the initial voltage of each ramp.

A prototype image sensor was realized in a 0.25µm CMOS process (Fig. 28.4.7). The pixel array has 400×330 3T pixels, with a pixel pitch of 7.4µm. The supply voltage is 2.5V for the analog and digital circuits and 3.3V for the I/O and analog switches. For flexibility, the digital circuitry that controls the column circuitry and ramp generator is implemented off-chip in an FPGA. This enables the ADC to operate in both the single-slope and MRSS modes, allowing for comparisons between the two architectures. The ADC's performance can be separately evaluated using a test input that feeds a common input signal to all columns. Figure 28.4.4 shows a measurement of the averaged INL at a clock frequency of 1MHz, both before and after the auto-calibration of the ramp generators is switched on. It clearly demonstrates the effectiveness of the auto-calibration scheme. Figure 28.4.5 shows a measured image at 50fps with the column ADC in 10b single-slope mode. At a clock frequency of 20MHz, the line time is 58µs, of which 53µs is used for the A/D conversion. Figure 28.4.6 shows a measured image at 142fps with the column ADC in 10b MRSS mode. The A/D conversion is now performed in 16µs, reducing the line time to 21µs. The power consumption of the analog circuit is 38mW, of which 30mW is used by the column CDS amplifiers and comparators and 8mW by the ramp generator.

In conclusion, a CMOS image sensor with a multiple-ramp single-slope ADC is presented. Compared to a single-slope ADC, it achieves a 3.3× decrease in conversion time, with a power increase of about 24%, and thus shows the potential of this new ADC architecture to increase power efficiency, speed, and chip area of column-level ADCs.

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References:
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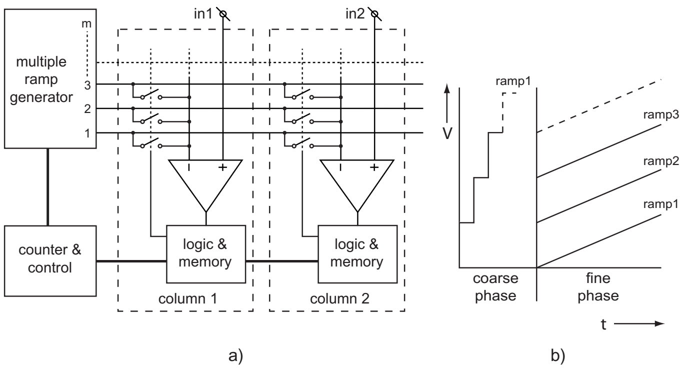

Figure 28.4.1: a) Block diagram of the multiple-ramp single-slope ADC architecture; b) Corresponding timing diagram.

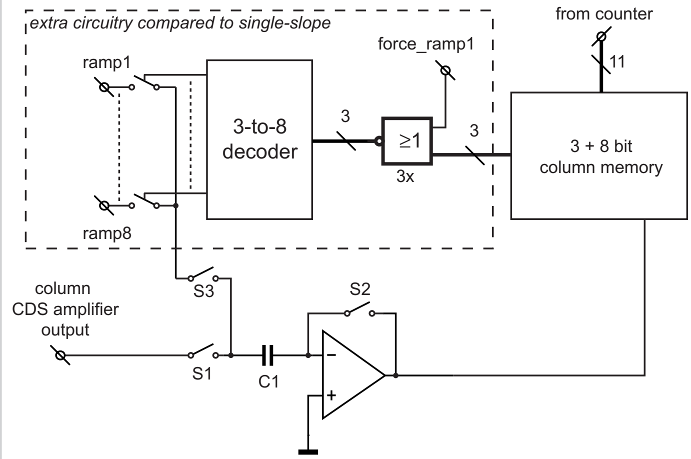

Figure 28.4.2: Simplified column-level ADC circuitry.

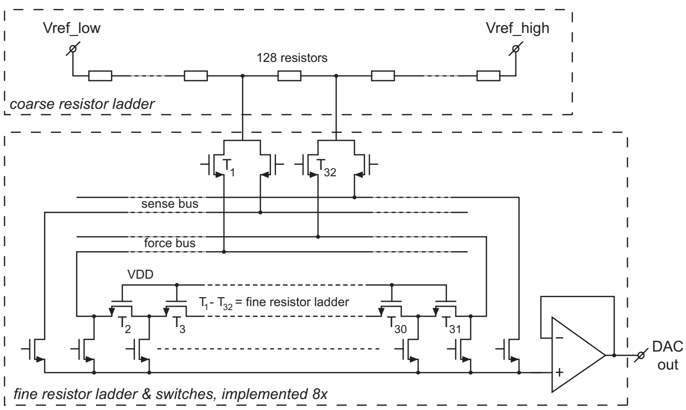

Figure 28.4.3: Circuit diagram of the multiple-ramp generator.

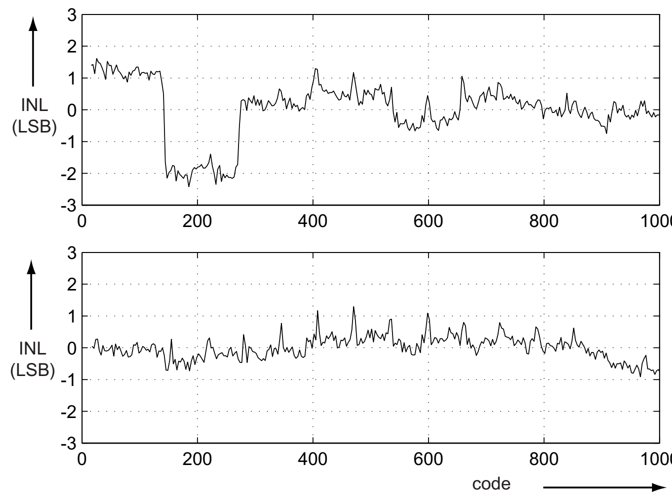

Figure 28.4.4: Measured averaged INL at 1MHz. a) without auto-calibration b) with auto-calibration

Figure 28.4.5: Image captured with the column ADC in single-slope mode at 50fps.

Figure 28.4.6: Image captured with the column ADC in MRSS mode at 142fps.

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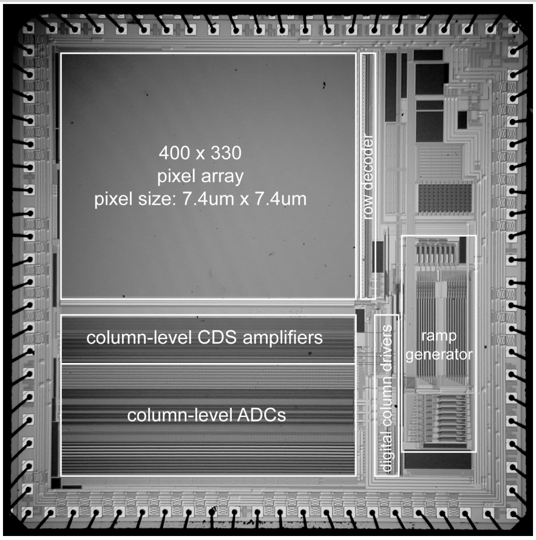

Figure 28.4.7: Chip micrograph of the prototype image sensor. The die size is 5mm x 5mm.

